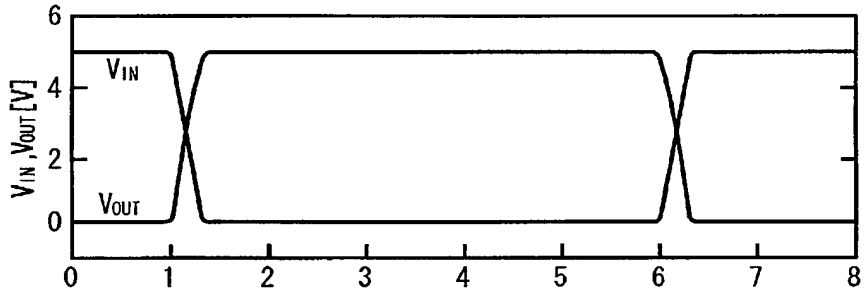


FIG. 1A

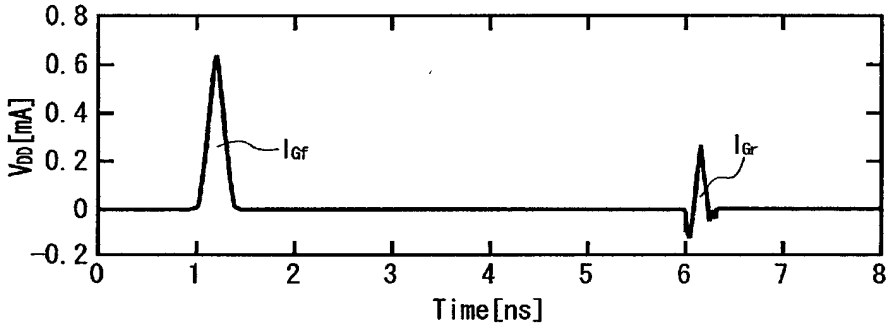


FIG. 1B

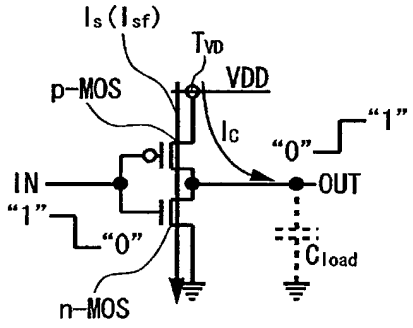


FIG. 1C

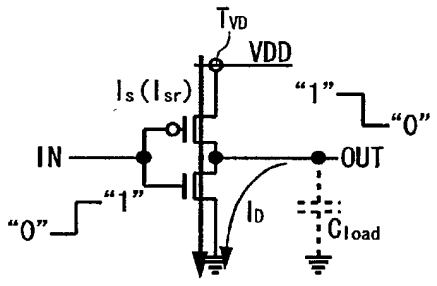


FIG. 1D

FIG. 2A

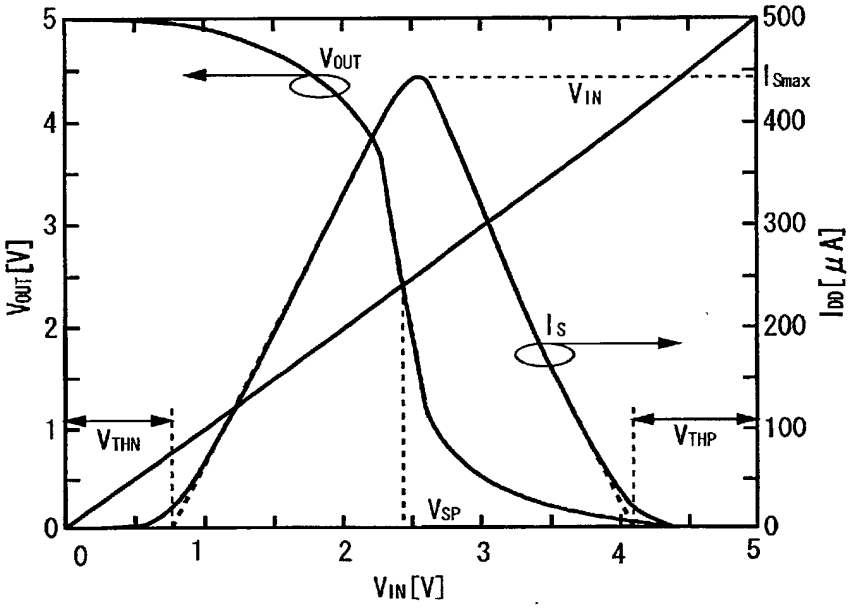

VOUT
VIN
ISmax
IS
VTHN
VTHP
VSP
VOUT[V]
IDD[μA]
VIN[V]
0
1
2
3
4
5
100
200
300
400
500

FIG. 2B

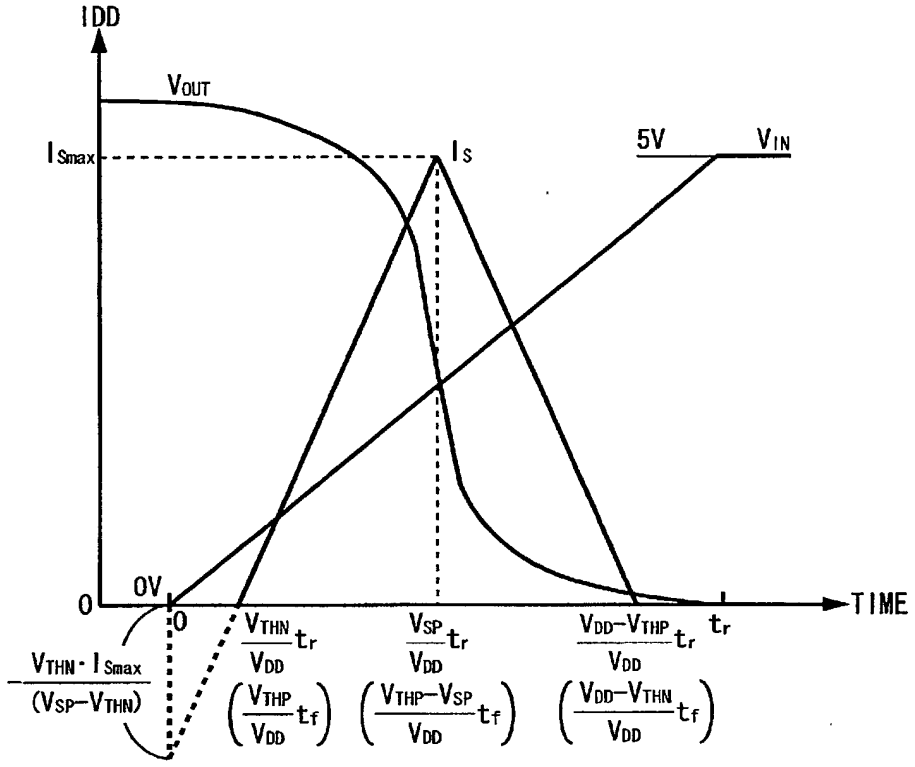

IDD
VOUT
ISmax
IS
5V
VIN
0V
0
TIME
$-\frac{V_{THN} \cdot I_{Smax}}{(V_{SP}-V_{THN})}$
$\frac{V_{THN}}{V_{DD}} t_r$
$\left(\frac{V_{THP}}{V_{DD}} t_f\right)$
$\frac{V_{SP}}{V_{DD}} t_r$
$\left(\frac{V_{THP}-V_{SP}}{V_{DD}} t_f\right)$
$\frac{V_{DD}-V_{THP}}{V_{DD}} t_r$
t_r
$\left(\frac{V_{DD}-V_{THN}}{V_{DD}} t_f\right)$

FIG. 3A

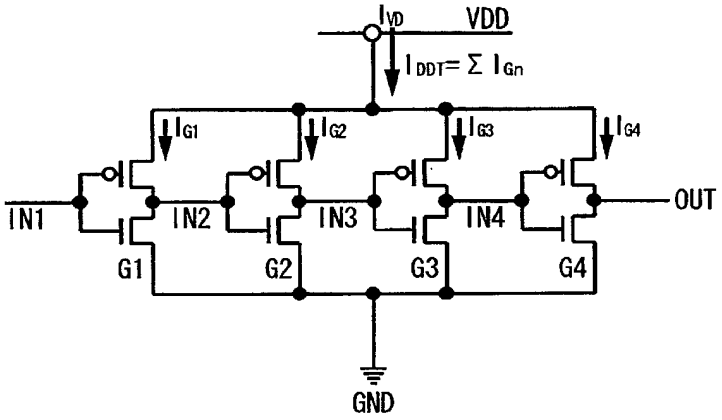


FIG. 3B

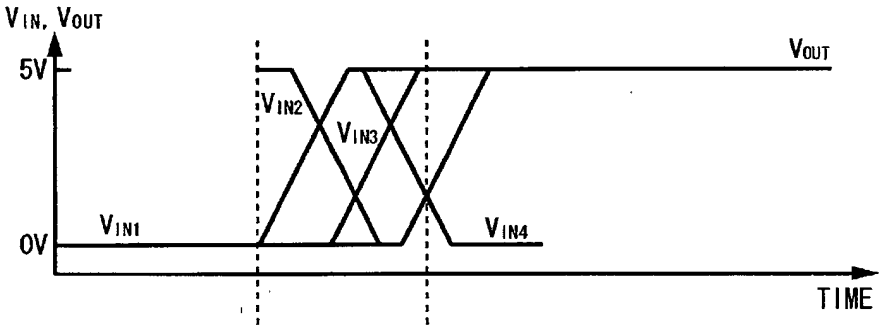
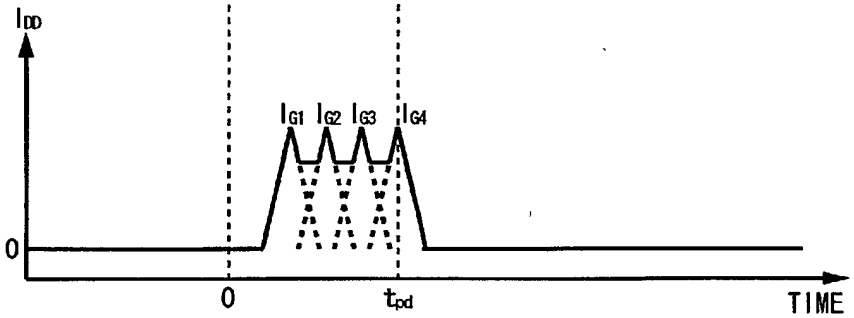


FIG. 3C



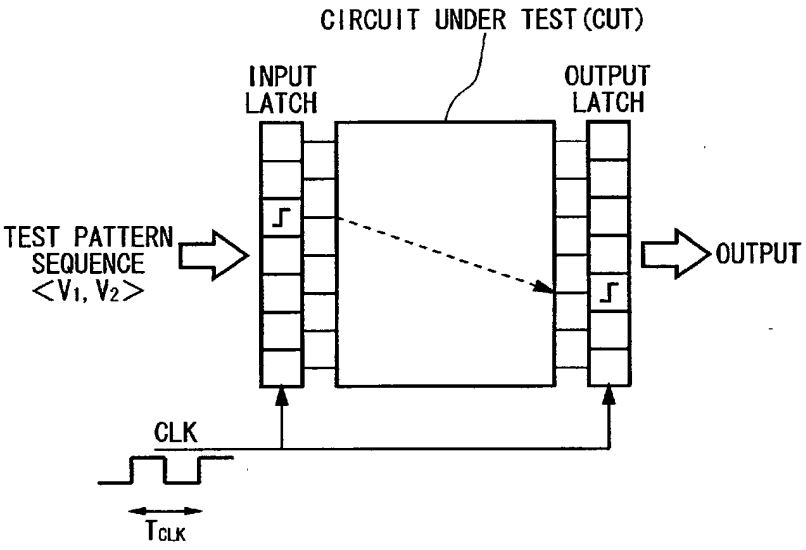

CIRCUIT UNDER TEST (CUT)
INPUT LATCH
OUTPUT LATCH
TEST PATTERN SEQUENCE <V1, V2>
OUTPUT
CLK
TCLK

FIG. 4A

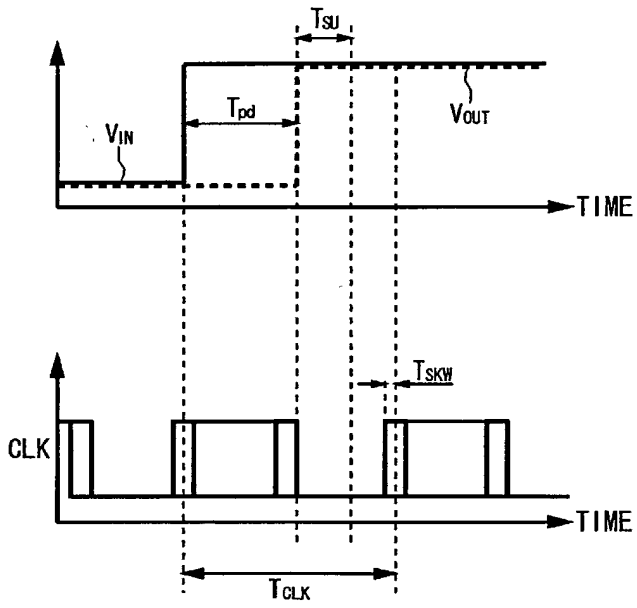

TSU
Tpd
VIN
VOUT
TIME
TSKW
CLK
TIME
TCLK

FIG. 4B

FIG. 5A

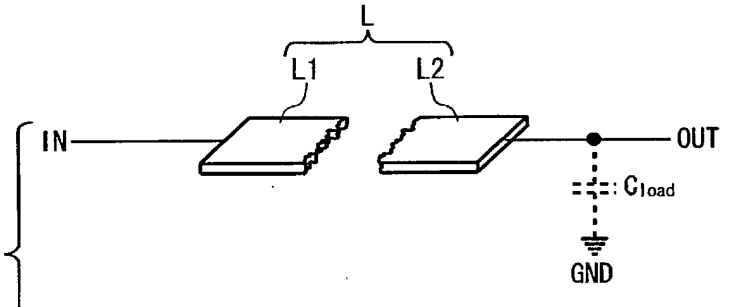


FIG. 5B

FIG. 5C

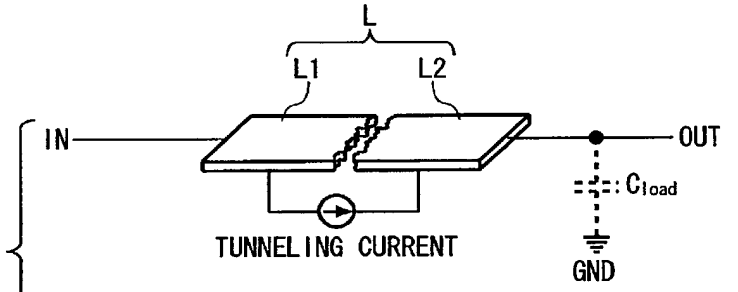


FIG. 5D

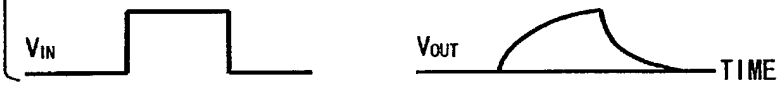


FIG. 6A

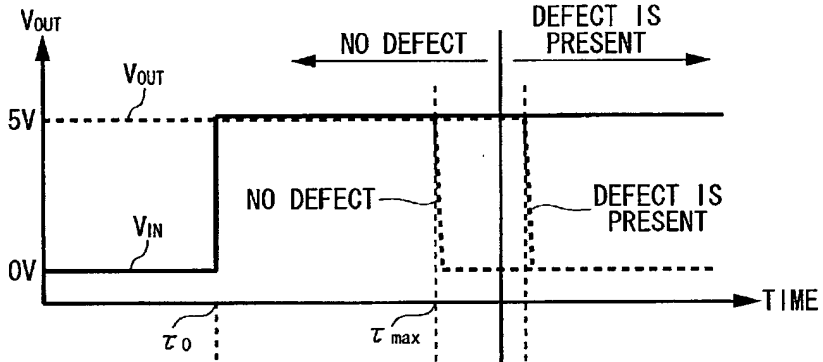

VOUT
NO DEFECT
DEFECT IS PRESENT
VOUT
5V
VIN
0V
NO DEFECT
DEFECT IS PRESENT
TIME
τ0
τ max

FIG. 6B

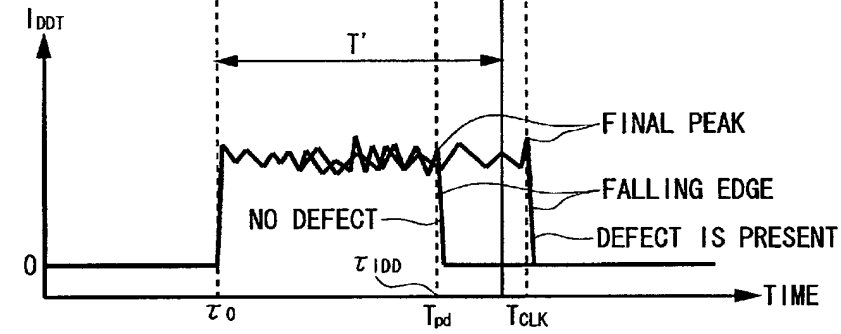

IDDT
T'
FINAL PEAK
FALLING EDGE
NO DEFECT
DEFECT IS PRESENT
0
τ IDD
TIME
τ0
Tpd
TCLK

FIG. 7A

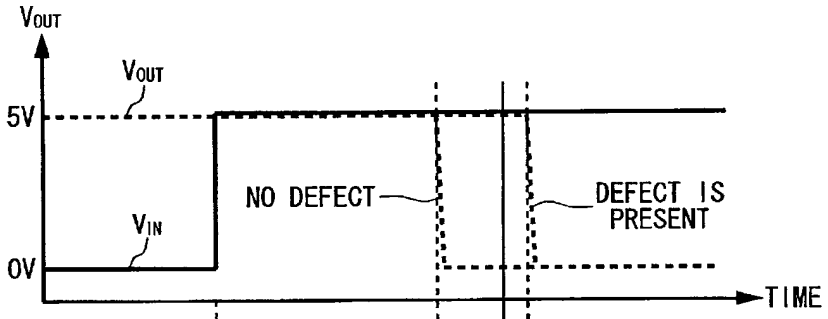
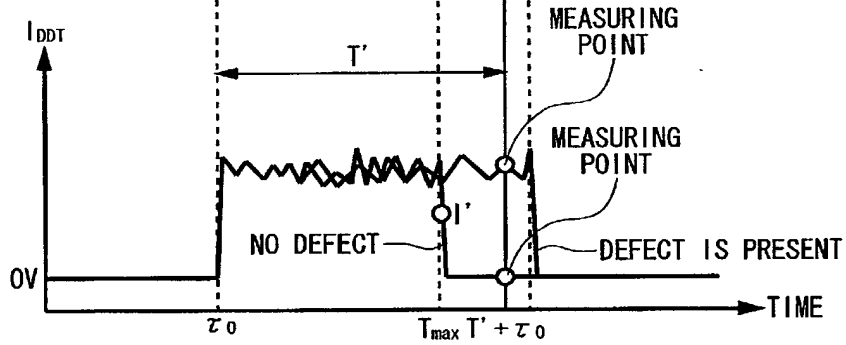


FIG. 7B



NO DEFECT: $i_{DDT}(T' + \tau_0) \leqq I'$

DEFECT IS PRESENT: $i_{DDT}(T' + \tau_0) > I'$

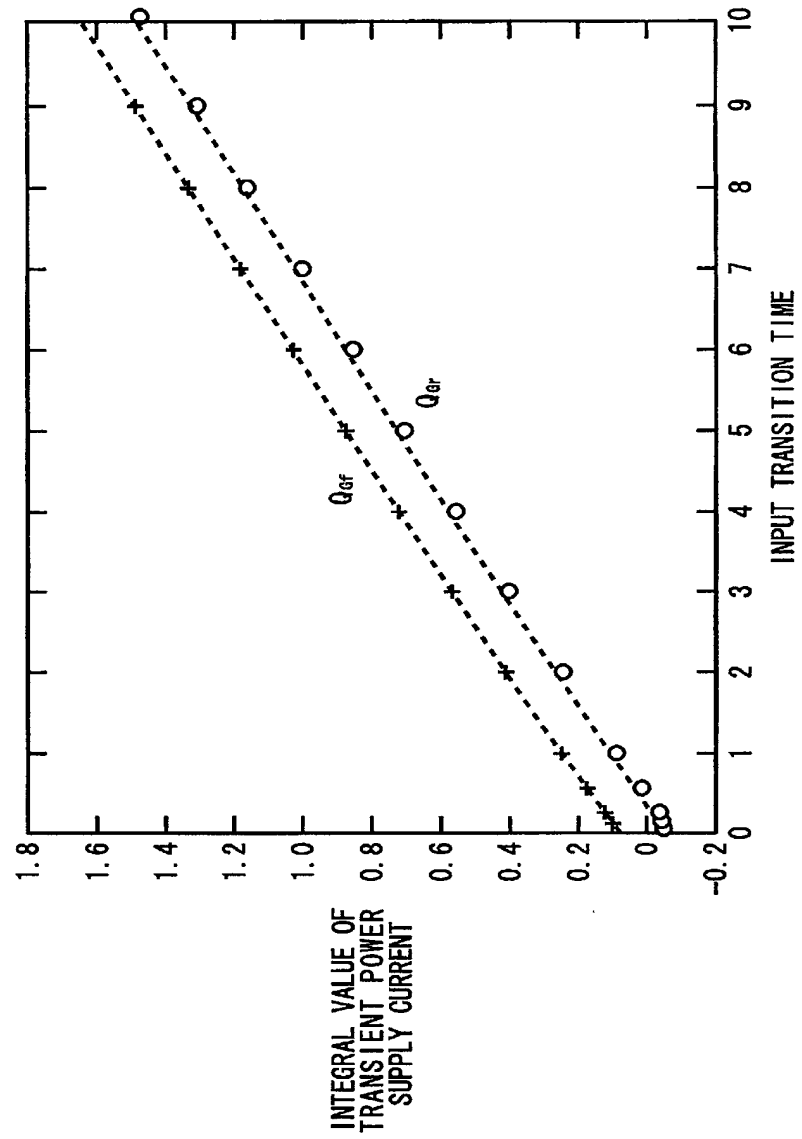

INTEGRAL VALUE OF TRANSIENT POWER SUPPLY CURRENT
INPUT TRANSITION TIME
Q_{Gf}
Q_{Gr}
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
-0.2
0
1
2
3
4
5
6
7
8
9
10

FIG. 8

FIG. 9A

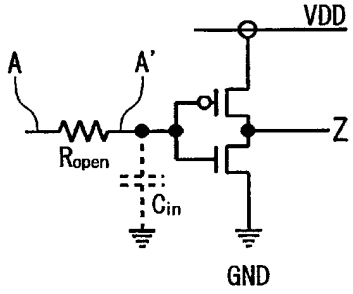


FIG. 9B

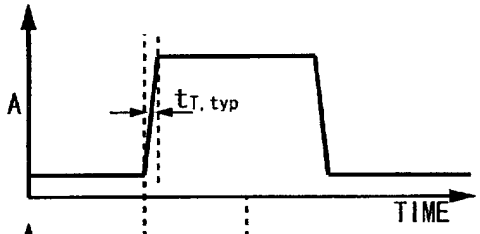
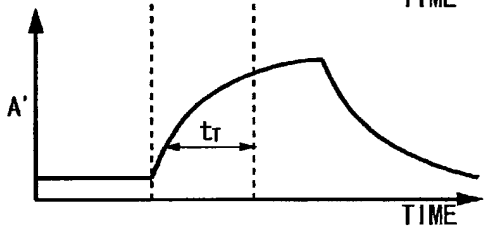


FIG. 9C



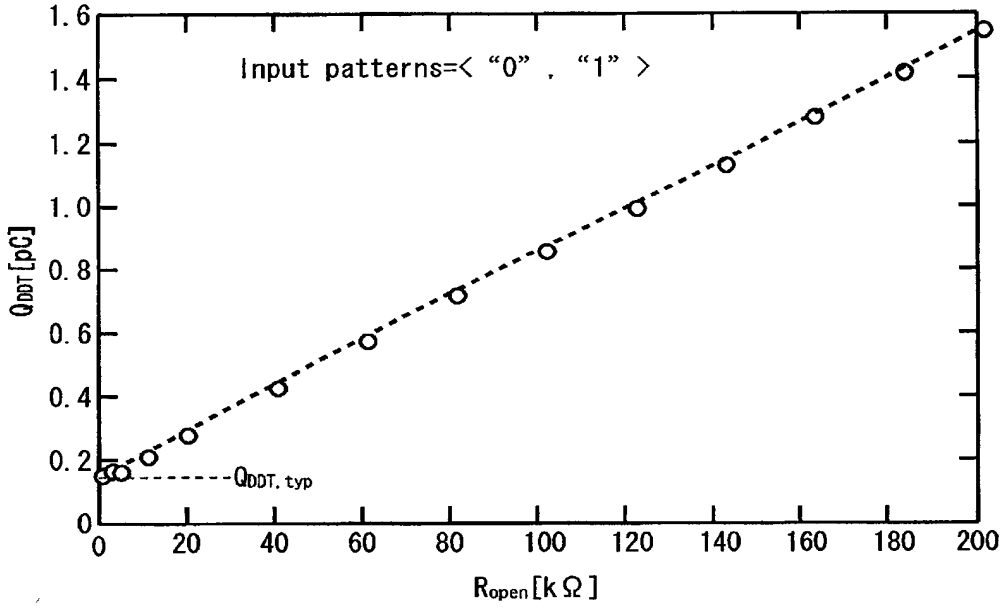

Input patterns=< "0" , "1" >
Q_{DDT}[pC]
R_{open}[kΩ]
$Q_{DDT.typ}$
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
0
20
40
60
80
100
120
140
160
180
200

FIG. 10

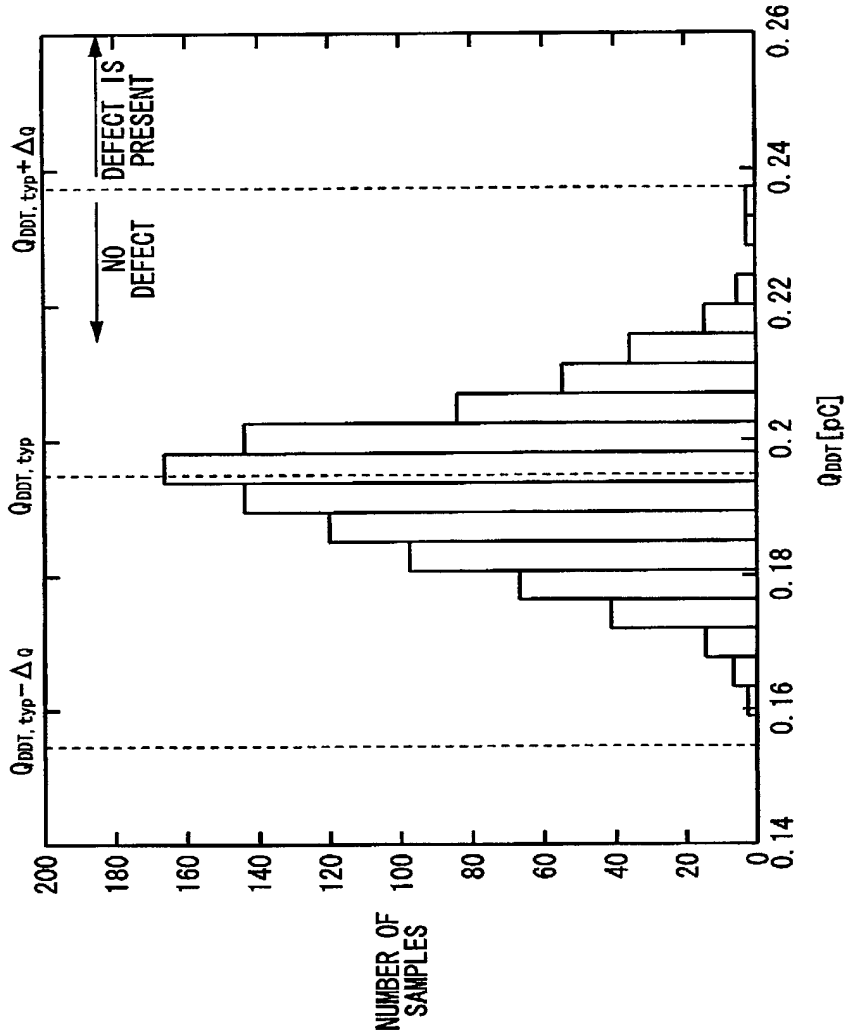

DEFECT IS PRESENT
NO DEFECT
$Q_{DDT, typ}+\Delta Q$
$Q_{DDT, typ}$
$Q_{DDT, typ}-\Delta Q$
NUMBER OF SAMPLES
Q_{DDT}[pC]
0
20
40
60
80
100
120
140
160
180
200
0.14
0.16
0.18
0.2
0.22
0.24
0.26

FIG. 11

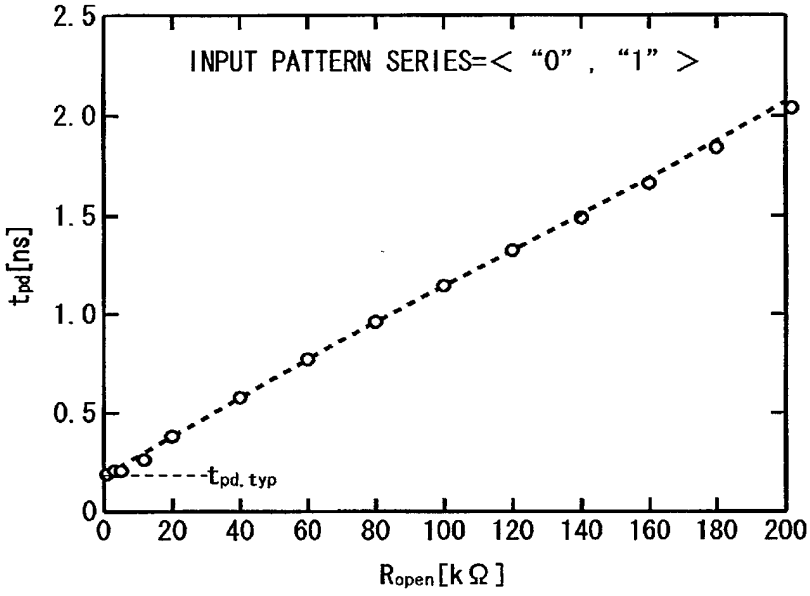

INPUT PATTERN SERIES=< "0" , "1" >
t_{pd}[ns]
$t_{pd, typ}$
R_{open}[k Ω]
2.5
2.0
1.5
1.0
0.5
0
0 20 40 60 80 100 120 140 160 180 200

FIG. 12

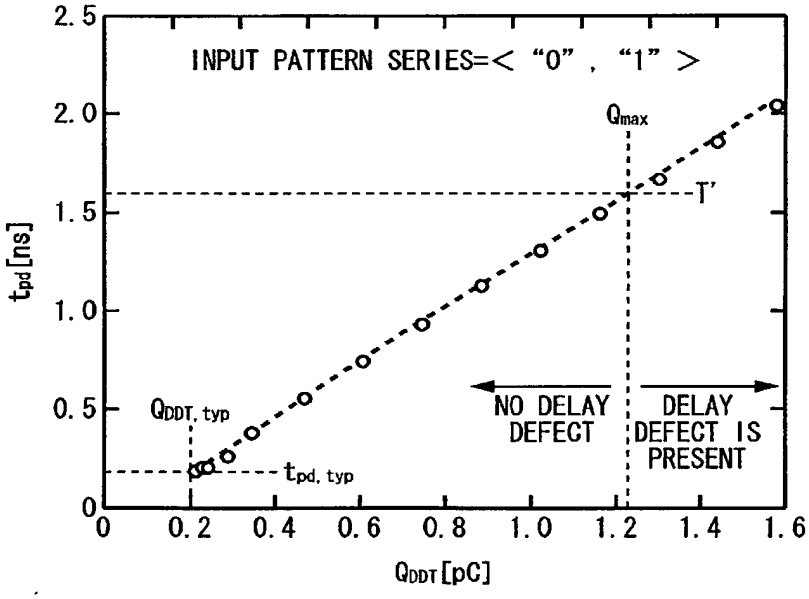

INPUT PATTERN SERIES=< "0" , "1" >
Q_{max}
T'
t_{pd}[ns]
$Q_{DDT, typ}$
$t_{pd, typ}$
NO DELAY DEFECT
DELAY DEFECT IS PRESENT
Q_{DDT}[pC]
2.5
2.0
1.5
1.0
0.5
0
0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6

FIG. 13

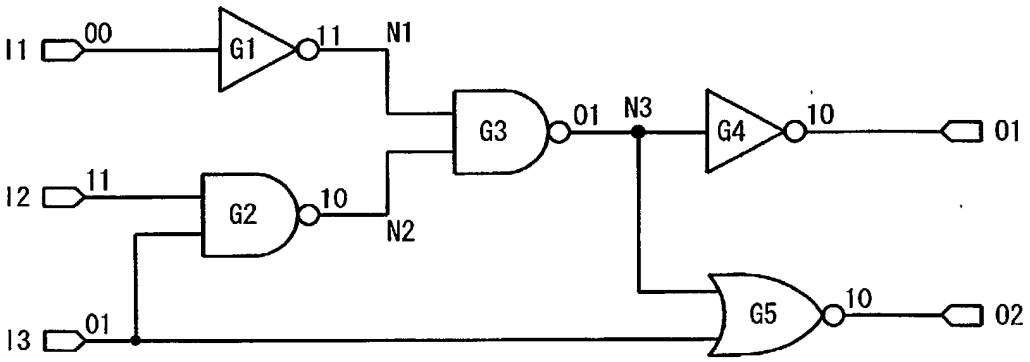


FIG. 14

FEDERAL EXPRESS

TEST PATTERN SEQUENCE ID NO.	INPUT TERMINAL			INTERNAL NODE			OUTPUT TERMINAL		DETECTABLE FAULTY GATE
	I1	I2	I3	N1	N2	N3	O1	O2	
T1	0	0	R	1	1	0	1	F	G5
T2	0	1	R	1	F	R	F	F	G2, G3, G4, G5
T3	1	0	R	0	1	1	0	0	——
T4	1	1	R	0	F	1	0	0	G2
T5	0	R	0	1	1	0	1	1	——
T6	0	R	1	1	F	R	F	0	G2, G3, G4
T7	1	R	0	0	1	1	0	0	——
T8	1	R	1	0	F	1	0	0	G2
T9	R	0	0	F	1	R	F	F	G1, G3, G4, G5
T10	R	0	1	F	1	R	F	0	G1, G3, G4
T11	R	1	0	F	1	R	F	F	G1, G3, G4, G5
T12	R	1	1	F	0	1	0	0	G1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 15

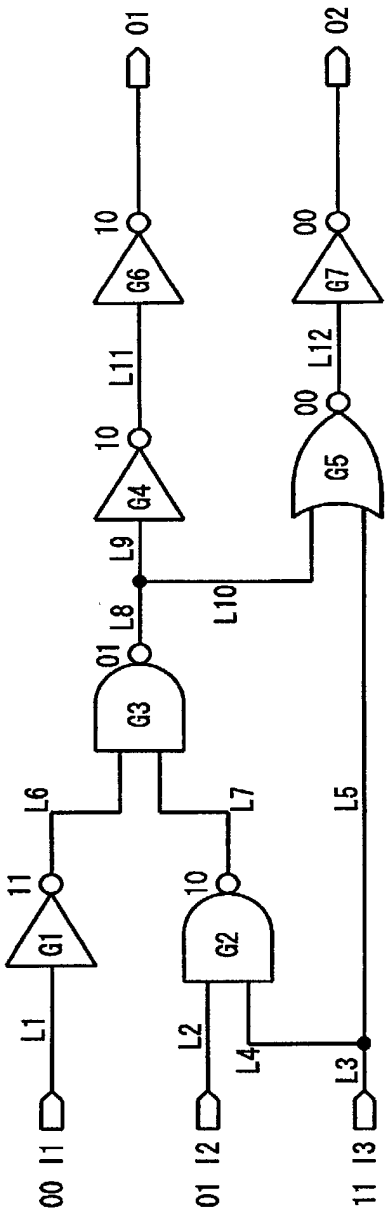

00 I1
01 I2
11 I3
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
G1
G2
G3
G4
G5
G6
G7
11
10
01
10
00
00
10
00
O1
O2

FIG. 16

TEST PATTERN SEQUENCE ID NO.	INPUT TERMINAL			INTERNAL SIGNAL LINE												OUTPUT TERMINAL		DETECTABLE DEFECTIVE INTERNAL SIGNAL LINE
	I1	I2	I3	1	2	3	4	5	6	7	8	9	10	11	12	O1	O2	
T1	0	0	R	0	0	R	R	R	1	1	1	1	1	1	F	1	F	L3, L5, L12
T2	0	1	R	0	1	R	R	R	1	F	F	F	F	F	F	F	F	L3, L4, L5, L7, L8, L9, L10, L11, L12
T3	1	0	R	1	0	R	R	R	0	1	0	0	0	0	0	0	0	——
T4	1	1	R	1	1	R	R	R	0	F	0	0	0	0	0	0	0	L3, L4
T5	0	R	0	0	R	0	0	0	1	1	1	1	1	1	1	1	1	——
T6	0	R	1	0	R	1	1	1	1	F	F	F	F	F	0	F	0	L2, L7, L8, L9, L11
T7	1	R	0	1	R	0	0	0	0	1	0	0	0	0	0	0	0	——
T8	1	R	1	1	R	1	1	1	0	F	0	0	0	0	0	0	0	L2
T9	R	0	0	R	0	0	0	0	F	1	F	F	F	F	F	F	F	L1, L6, L8, L9, L10, L11, L12
T10	R	0	1	R	0	1	1	1	F	1	F	F	F	F	0	F	0	L1, L6, L8, L9, L11
T11	R	1	0	R	1	0	0	0	F	1	F	F	F	F	F	F	F	L1, L6, L8, L9, L10, L11, L12
T12	R	1	1	R	1	1	1	1	F	0	0	0	0	0	0	0	0	L1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 17

US 7,818,651 B2

TEST PATTERN SEQUENCE ID NO.	INPUT SIGNAL			INTERNAL NODE			OUTPUT TERMINAL		DETECTABLE FAULTY PATH
	I1	I2	I3	N1	N2	N3	O1	O2	
T1	0	0	R	1	1	0	1	F	<I3, O2>
T2	0	1	R	1	F	R	F	F	<I3, N2, N3, O1> <I3, N2, N3, O2>
T3	1	0	R	0	1	1	0	0	——
T4	0	1	R	0	F	1	0	0	——
T5	0	R	0	1	1	0	1	1	——
T6	0	R	1	1	F	R	F	0	<I2, N2, N3, O1>
T7	1	R	0	0	1	1	0	0	——
T8	1	R	1	0	F	1	0	0	——
T9	R	0	0	F	1	R	F	F	<I1, N1, N3, O1> <I1, N1, N3, O2>
T10	R	0	1	F	1	R	F	0	<I1, N1, N3, O1>
T11	R	1	0	F	1	R	F	F	<I1, N1, N3, O1> <I1, N1, N3, O2>
T12	R	1	1	F	0	1	0	0	——
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 18

TEST PATTERN SEQUENCE ID NO.	INPUT TERMINAL			INTERNAL SIGNAL LINE												OUTPUT TERMINAL		DETECTABLE FAULTY PATH
	I1	I2	I3	1	2	3	4	5	6	7	8	9	10	11	12	1	2	
T1	0	0	R	0	0	R	R	R	1	1	1	1	1	1	F	1	F	<I3, L3, L5, L12, O2>
T2	0	1	R	0	1	R	R	R	1	F	F	F	F	F	F	F	F	<I3, L3, L5, L12, O2> <I3, L3, L4, L7, L8, L9, L11, O1> <I3, L3, L4, L7, L8, L10, L12, O1>
T3	1	0	R	1	0	R	R	R	0	1	0	0	0	0	0	0	0	—
T4	1	1	R	1	1	R	R	R	0	F	0	0	0	0	0	0	0	—
T5	0	R	0	0	R	0	0	0	1	1	1	1	1	1	1	1	1	—
T6	0	R	1	0	R	1	1	1	1	F	F	F	F	F	F	F	0	<I2, L2, L7, L8, L9, L11, O1>
T7	1	R	0	1	R	0	0	0	0	1	0	0	0	0	0	0	0	—
T8	1	R	1	1	R	1	1	1	0	F	0	0	0	0	0	0	0	—
T9	R	0	0	R	0	0	0	0	F	1	F	F	F	F	F	F	F	<I1, L1, L6, L8, L9, L11, O1> <I1, L1, L6, L8, L10, L12, O2>
T10	R	0	1	R	0	1	1	1	F	1	F	F	F	F	0	F	0	<I1, L1, L6, L8, L9, L11, O1>
T11	R	1	0	R	1	0	0	0	F	1	F	F	F	F	F	F	F	<I1, L1, L6, L8, L9, L11, O1> <I1, L1, L6, L8, L10, L12, O2>
T12	R	1	1	R	1	1	1	1	F	0	0	0	0	0	0	0	0	—
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 19

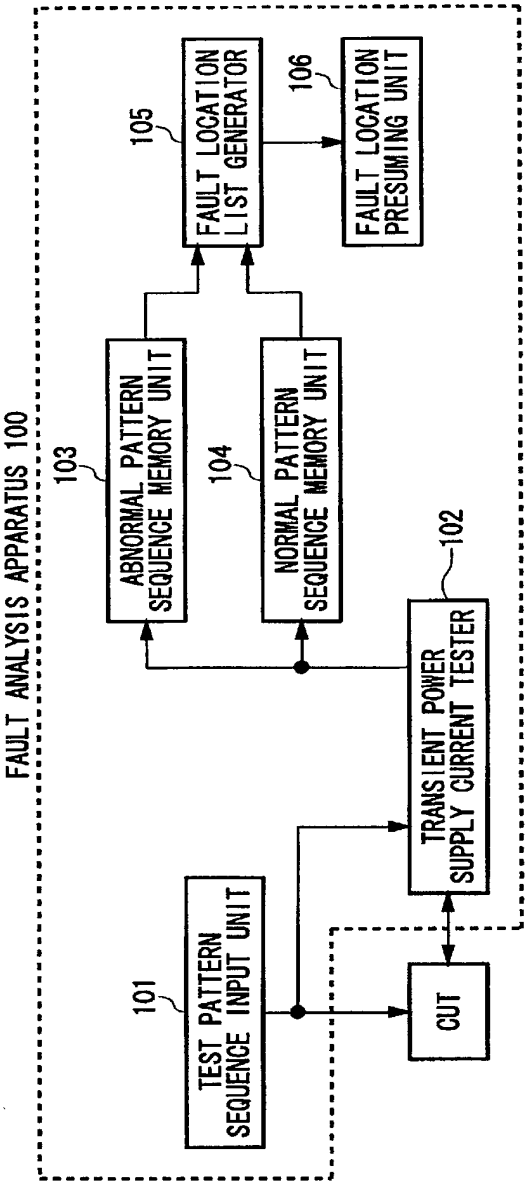

FAULT ANALYSIS APPARATUS 100
TEST PATTERN SEQUENCE INPUT UNIT
101
ABNORMAL PATTERN SEQUENCE MEMORY UNIT
103
NORMAL PATTERN SEQUENCE MEMORY UNIT
104
FAULT LOCATION LIST GENERATOR
105
FAULT LOCATION PRESUMING UNIT
106
TRANSIENT POWER SUPPLY CURRENT TESTER
102
CUT

FIG. 20

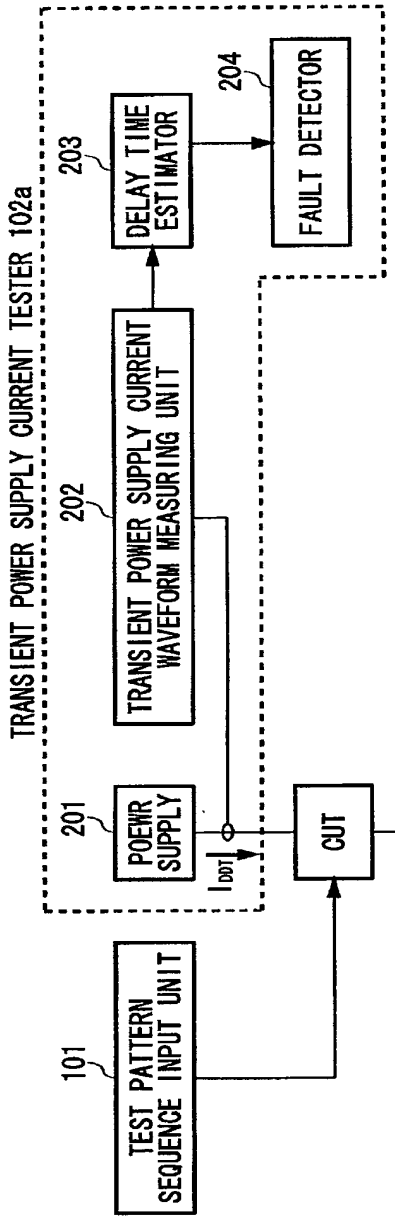

TRANSIENT POWER SUPPLY CURRENT TESTER 102a
101
TEST PATTERN SEQUENCE INPUT UNIT
201
POEWR SUPPLY
I_{DDT}
CUT
GND
202
TRANSIENT POWER SUPPLY CURRENT WAVEFORM MEASURING UNIT
203
DELAY TIME ESTIMATOR
204
FAULT DETECTOR

FIG. 21

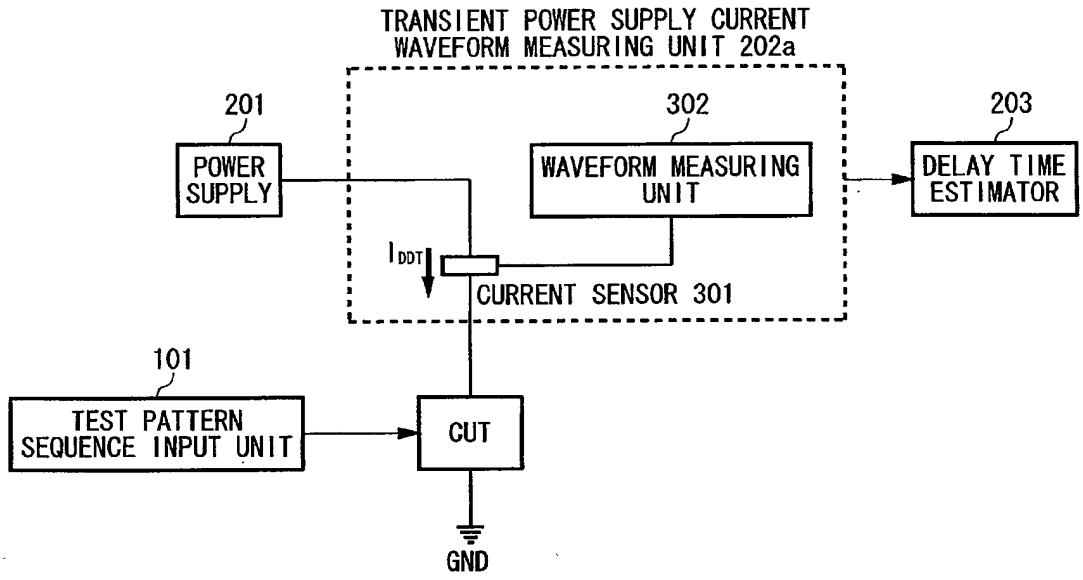

TRANSIENT POWER SUPPLY CURRENT
WAVEFORM MEASURING UNIT 202a
201
POWER SUPPLY
302
WAVEFORM MEASURING UNIT
203
DELAY TIME ESTIMATOR
I_{DDT}
CURRENT SENSOR 301
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
GND

FIG. 22

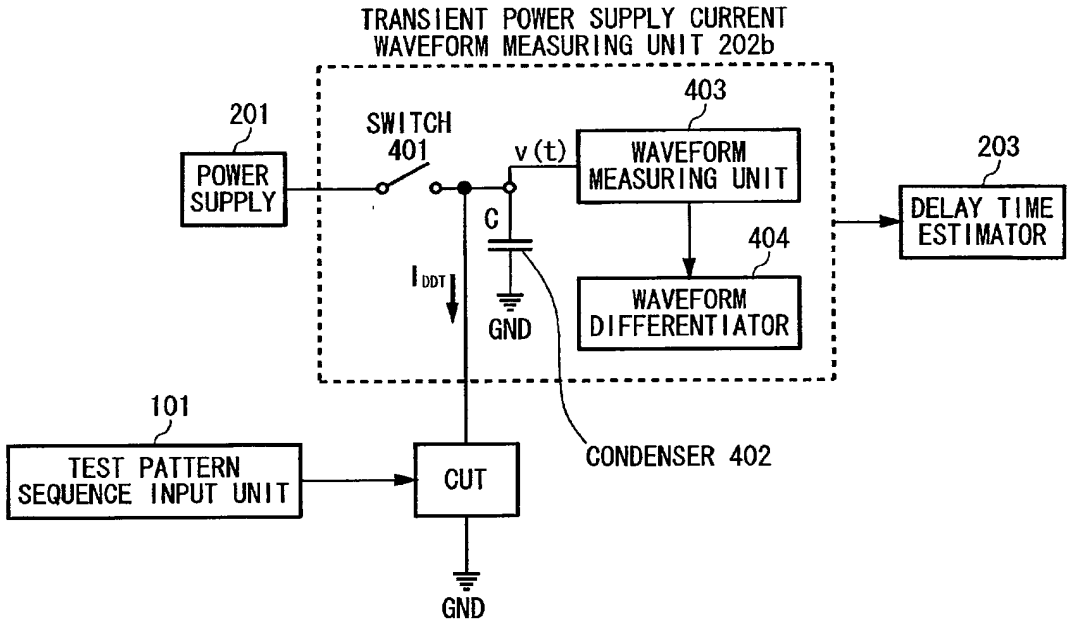

TRANSIENT POWER SUPPLY CURRENT
WAVEFORM MEASURING UNIT 202b
201
POWER SUPPLY
SWITCH
401
v(t)
403
WAVEFORM MEASURING UNIT
203
DELAY TIME ESTIMATOR
C
404
WAVEFORM DIFFERENTIATOR
IDDT
GND
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
CONDENSER 402
GND

FIG. 23

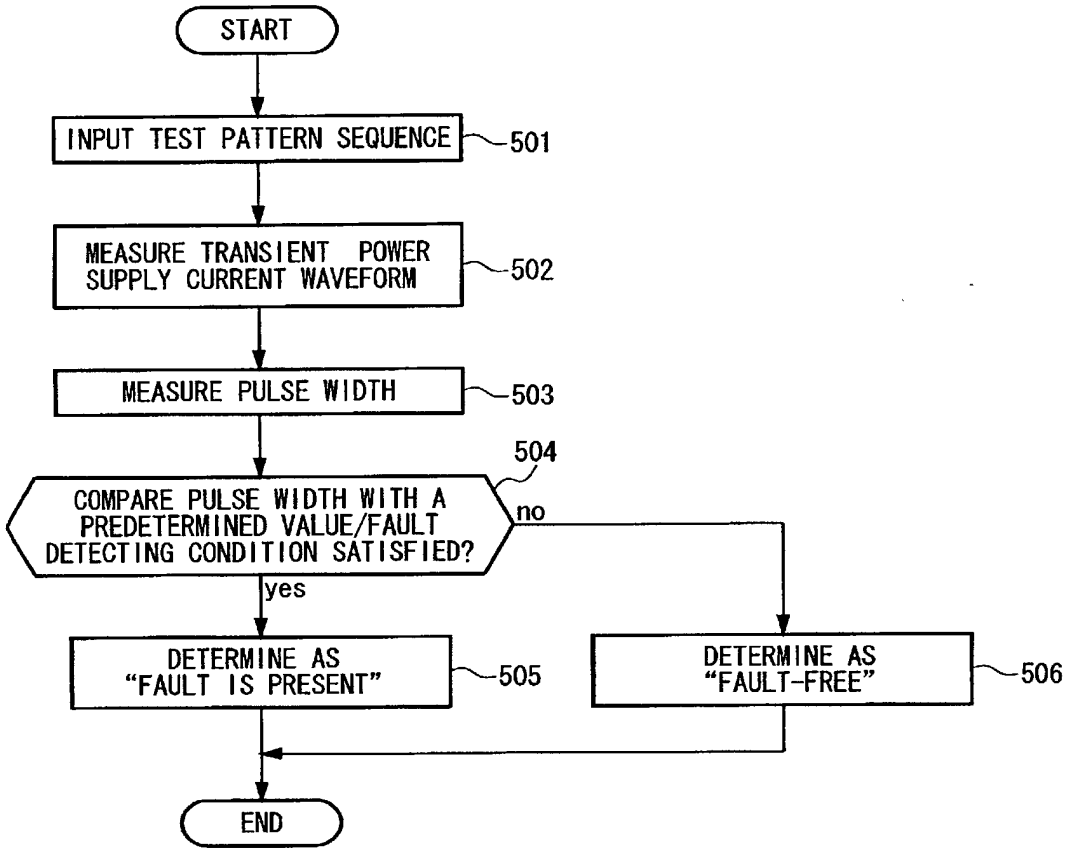

START
INPUT TEST PATTERN SEQUENCE
501
MEASURE TRANSIENT POWER SUPPLY CURRENT WAVEFORM
502
MEASURE PULSE WIDTH
503
504
COMPARE PULSE WIDTH WITH A PREDETERMINED VALUE/FAULT DETECTING CONDITION SATISFIED?
no
yes
DETERMINE AS "FAULT IS PRESENT"
505
DETERMINE AS "FAULT-FREE"
506
END

FIG. 24

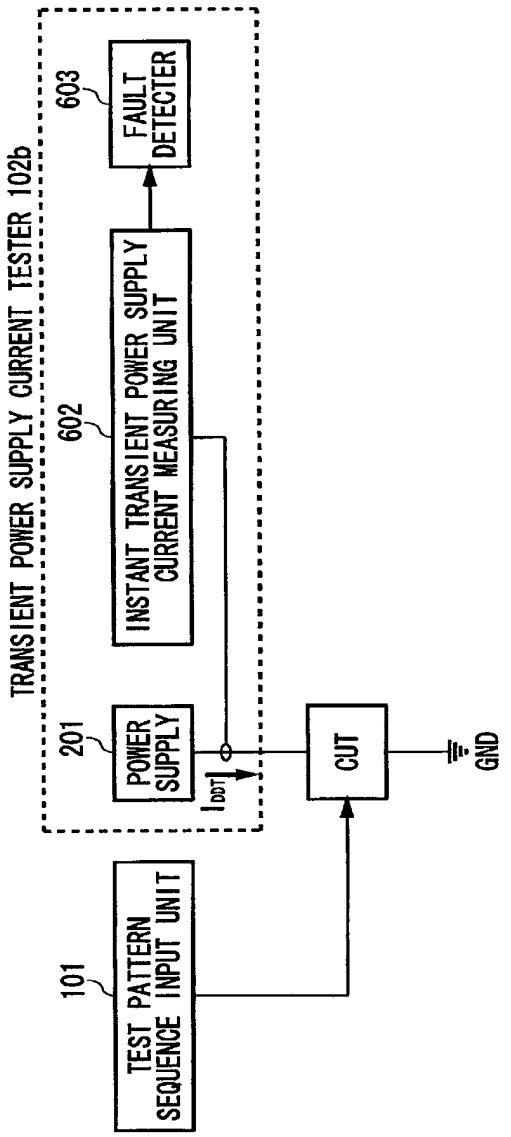

TRANSIENT POWER SUPPLY CURRENT TESTER 102b
603
FAULT DETECTER
602
INSTANT TRANSIENT POWER SUPPLY CURRENT MEASURING UNIT
201
POWER SUPPLY
I_{DDT}
CUT
GND
101
TEST PATTERN SEQUENCE INPUT UNIT

FIG. 25

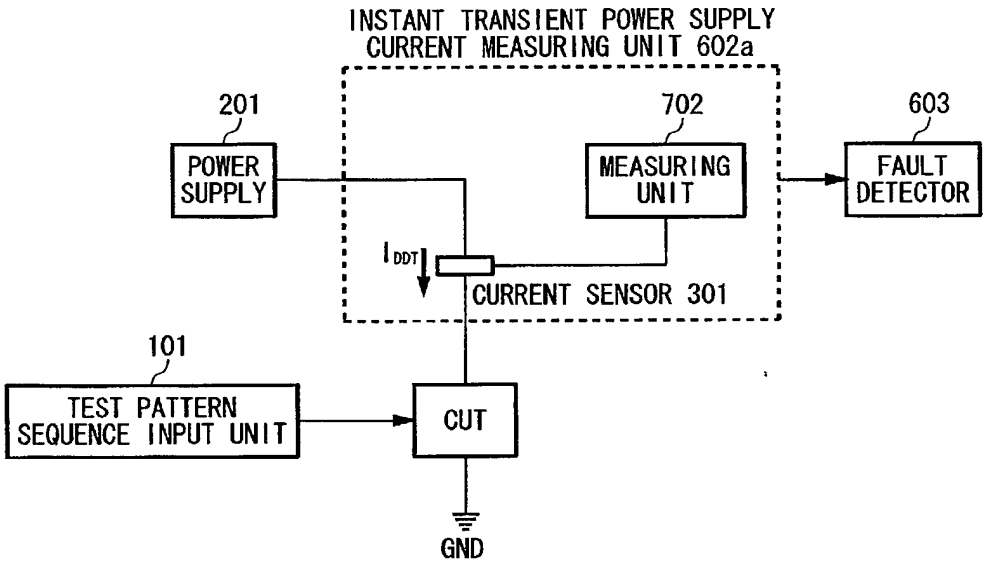

INSTANT TRANSIENT POWER SUPPLY CURRENT MEASURING UNIT 602a
201
POWER SUPPLY
702
MEASURING UNIT
603
FAULT DETECTOR
I_{DDT}
CURRENT SENSOR 301
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
GND

FIG. 26

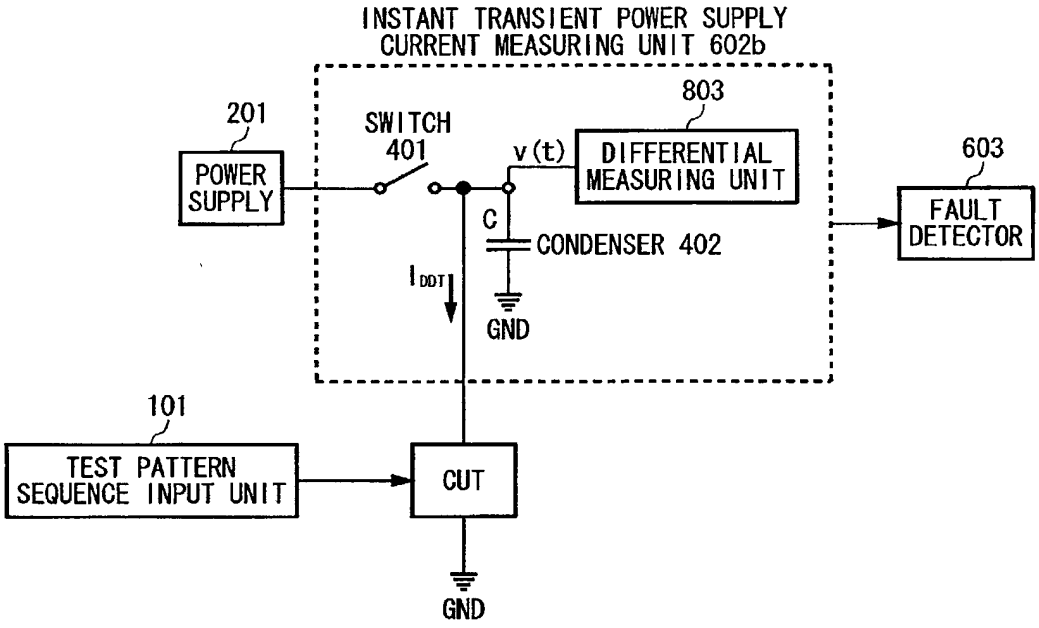

INSTANT TRANSIENT POWER SUPPLY CURRENT MEASURING UNIT 602b
201
POWER SUPPLY
SWITCH 401
803
v(t)
DIFFERENTIAL MEASURING UNIT
603
FAULT DETECTOR
C
CONDENSER 402
I_{DDT}
GND
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
GND

FIG. 27

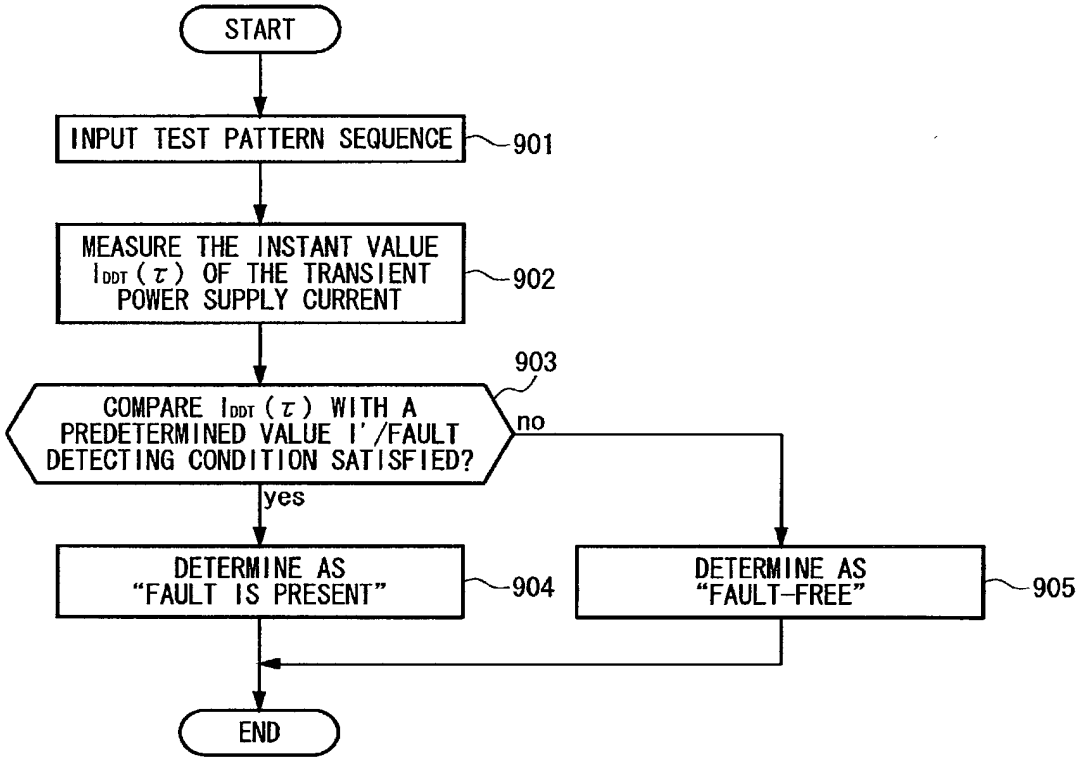

START
INPUT TEST PATTERN SEQUENCE
901
MEASURE THE INSTANT VALUE $I_{DDT}(\tau)$ OF THE TRANSIENT POWER SUPPLY CURRENT
902
903
COMPARE $I_{DDT}(\tau)$ WITH A PREDETERMINED VALUE I'/FAULT DETECTING CONDITION SATISFIED?
no
yes
DETERMINE AS "FAULT IS PRESENT"
904
DETERMINE AS "FAULT-FREE"
905
END

FIG. 28

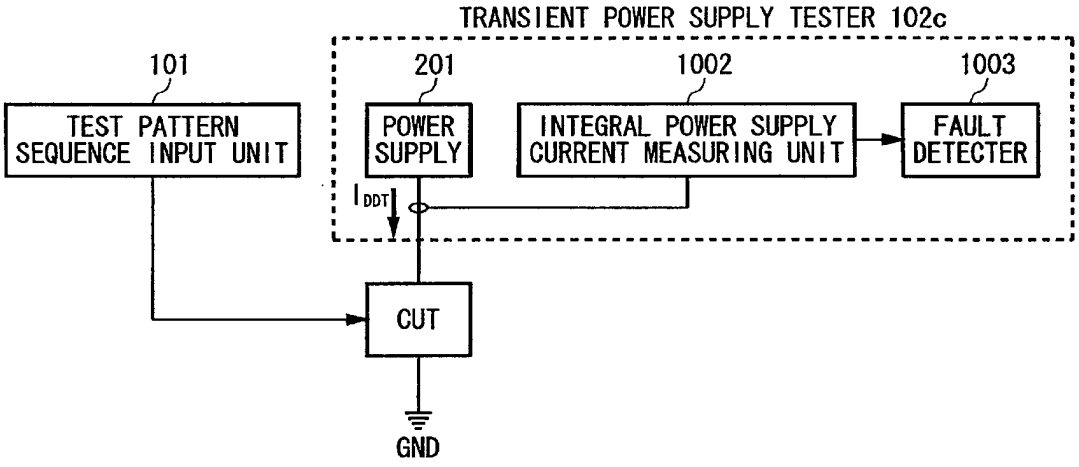

TRANSIENT POWER SUPPLY TESTER 102c
101
TEST PATTERN SEQUENCE INPUT UNIT
201
POWER SUPPLY
1002
INTEGRAL POWER SUPPLY CURRENT MEASURING UNIT
1003
FAULT DETECTER
IDDT
CUT
GND

FIG. 29

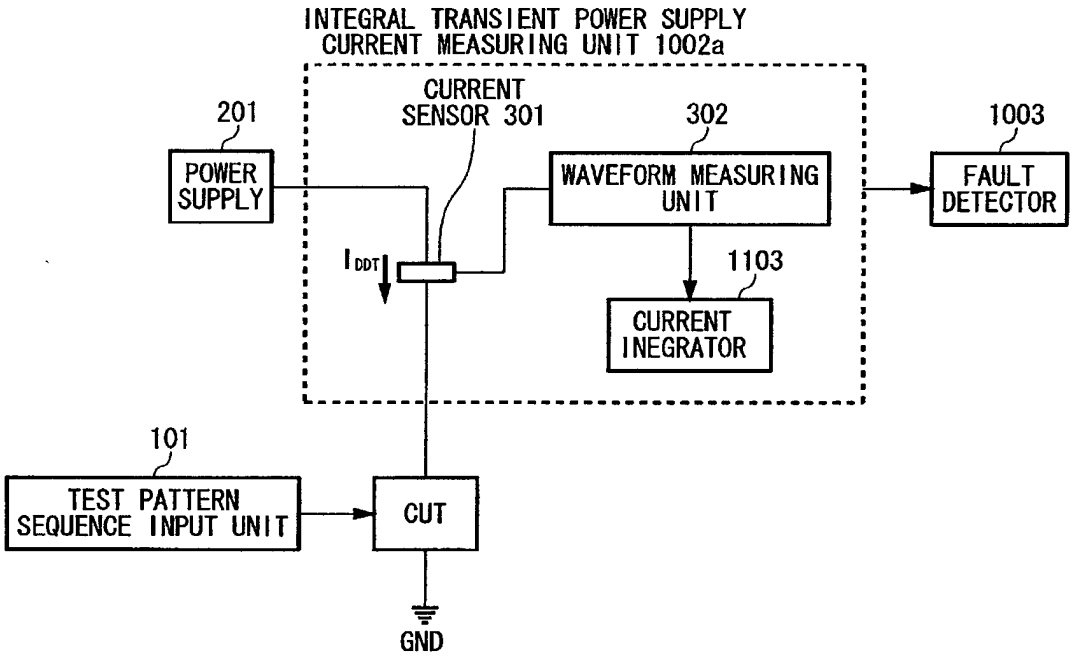

INTEGRAL TRANSIENT POWER SUPPLY CURRENT MEASURING UNIT 1002a
201
POWER SUPPLY
CURRENT SENSOR 301
302
WAVEFORM MEASURING UNIT
1003
FAULT DETECTOR
IDDT
1103
CURRENT INEGRATOR
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
GND

FIG. 30

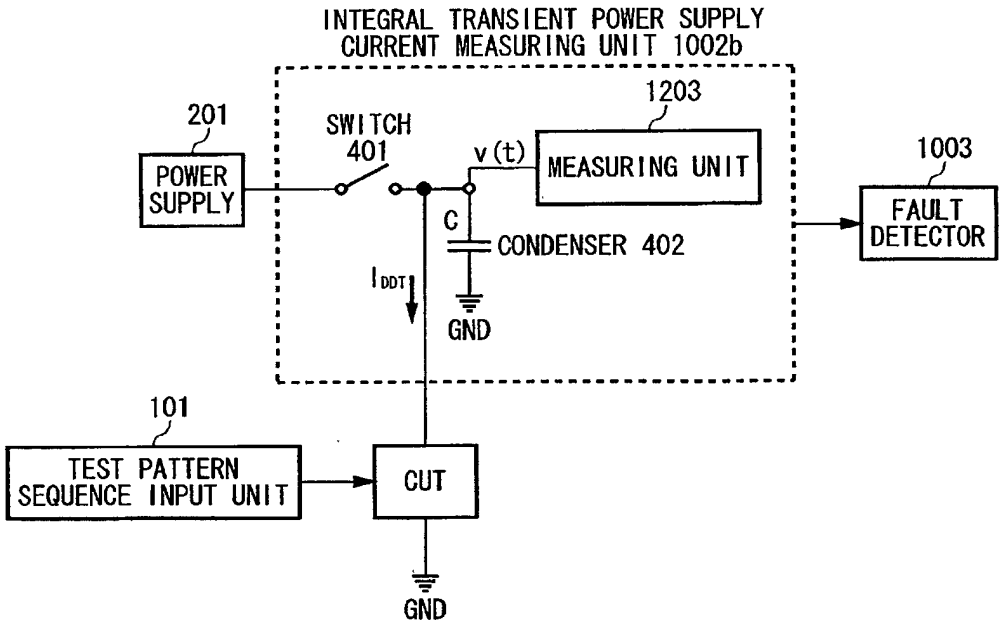

INTEGRAL TRANSIENT POWER SUPPLY CURRENT MEASURING UNIT 1002b
201
POWER SUPPLY
SWITCH 401
v(t)
1203
MEASURING UNIT
1003
FAULT DETECTOR
C
CONDENSER 402
I_{DDT}
GND
101
TEST PATTERN SEQUENCE INPUT UNIT
CUT
GND

FIG. 31

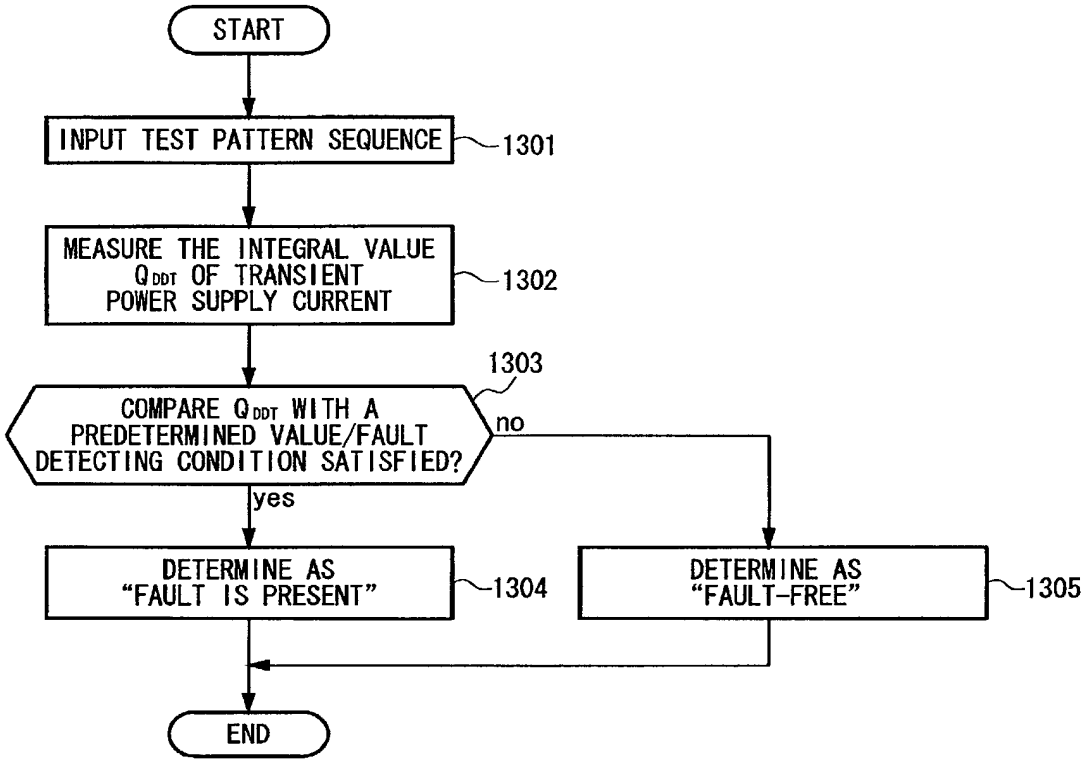

START
INPUT TEST PATTERN SEQUENCE
1301
MEASURE THE INTEGRAL VALUE Q_{DDT} OF TRANSIENT POWER SUPPLY CURRENT
1302
1303
COMPARE Q_{DDT} WITH A PREDETERMINED VALUE/FAULT DETECTING CONDITION SATISFIED?
no
yes
DETERMINE AS "FAULT IS PRESENT"
1304
DETERMINE AS "FAULT-FREE"
1305
END

FIG. 32

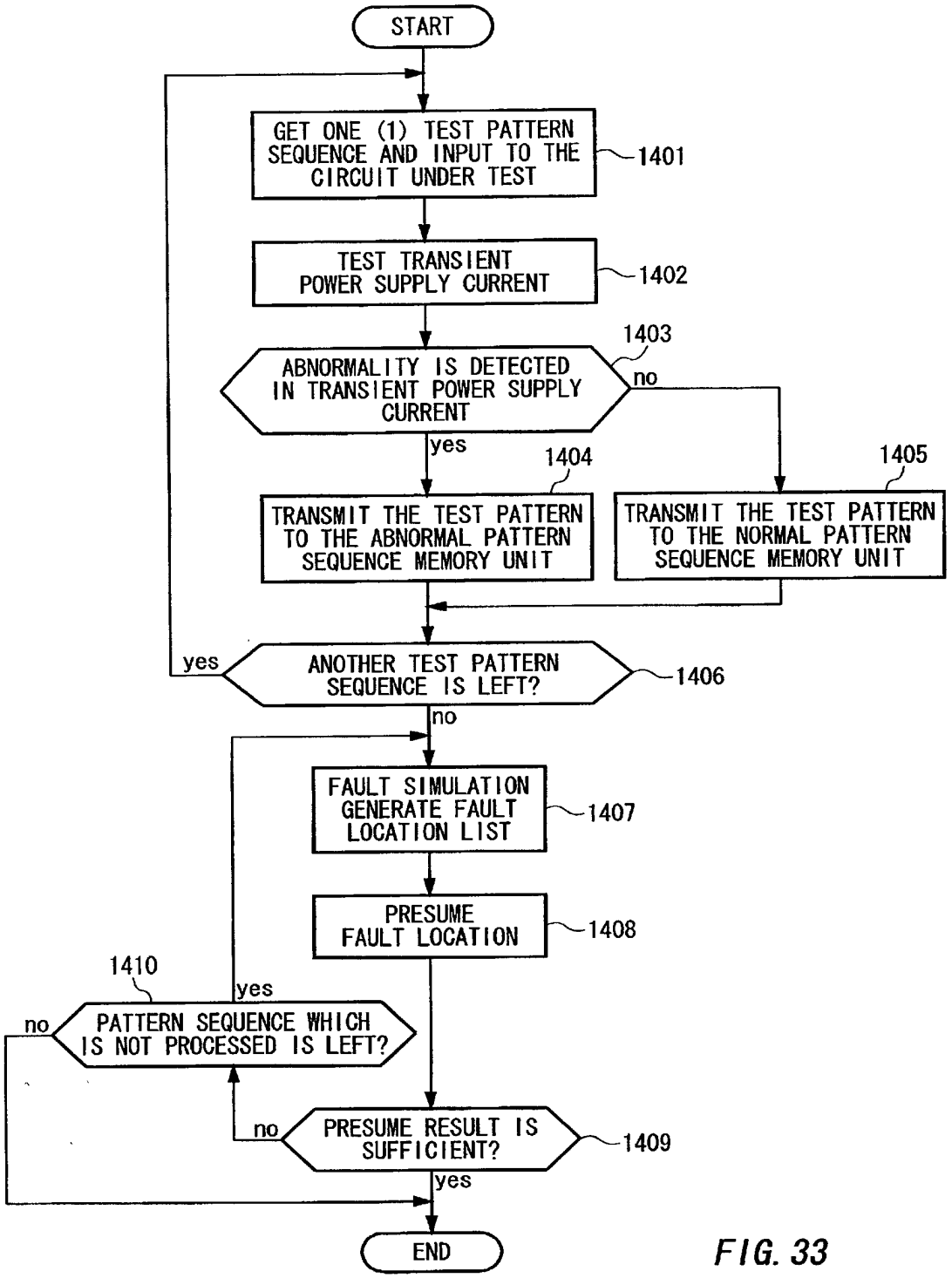

START
GET ONE (1) TEST PATTERN SEQUENCE AND INPUT TO THE CIRCUIT UNDER TEST
1401
TEST TRANSIENT POWER SUPPLY CURRENT
1402
ABNORMALITY IS DETECTED IN TRANSIENT POWER SUPPLY CURRENT
1403
no
yes
TRANSMIT THE TEST PATTERN TO THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
1404
TRANSMIT THE TEST PATTERN TO THE NORMAL PATTERN SEQUENCE MEMORY UNIT
1405
yes
ANOTHER TEST PATTERN SEQUENCE IS LEFT?
1406
no
FAULT SIMULATION GENERATE FAULT LOCATION LIST
1407
PRESUME FAULT LOCATION
1408
1410
yes
no
PATTERN SEQUENCE WHICH IS NOT PROCESSED IS LEFT?
no
PRESUME RESULT IS SUFFICIENT?
1409
yes
END

FIG. 33

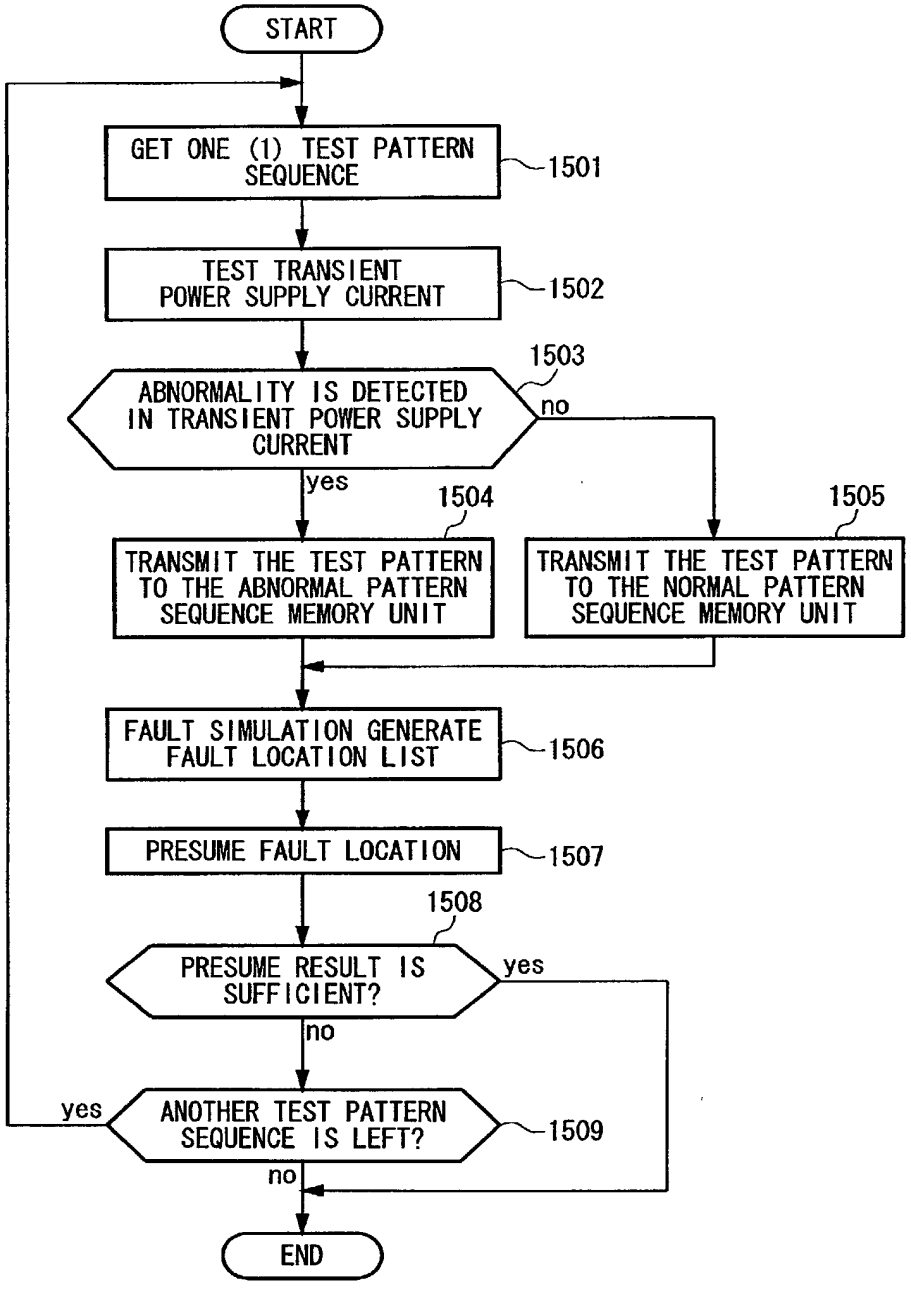

START
GET ONE (1) TEST PATTERN SEQUENCE
1501
TEST TRANSIENT POWER SUPPLY CURRENT
1502
1503
ABNORMALITY IS DETECTED IN TRANSIENT POWER SUPPLY CURRENT
no
yes
1504
TRANSMIT THE TEST PATTERN TO THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
1505
TRANSMIT THE TEST PATTERN TO THE NORMAL PATTERN SEQUENCE MEMORY UNIT
FAULT SIMULATION GENERATE FAULT LOCATION LIST
1506
PRESUME FAULT LOCATION
1507
1508
PRESUME RESULT IS SUFFICIENT?
yes
no
yes
ANOTHER TEST PATTERN SEQUENCE IS LEFT?
1509
no
END

FIG. 34

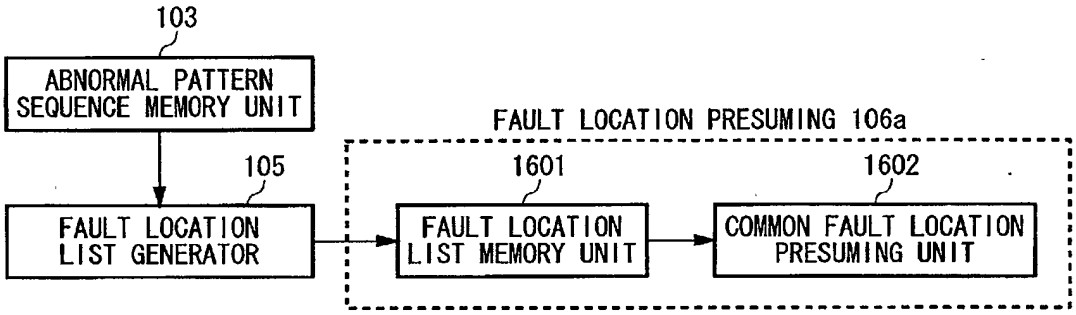


FIG. 35

TOSHIBA-000650

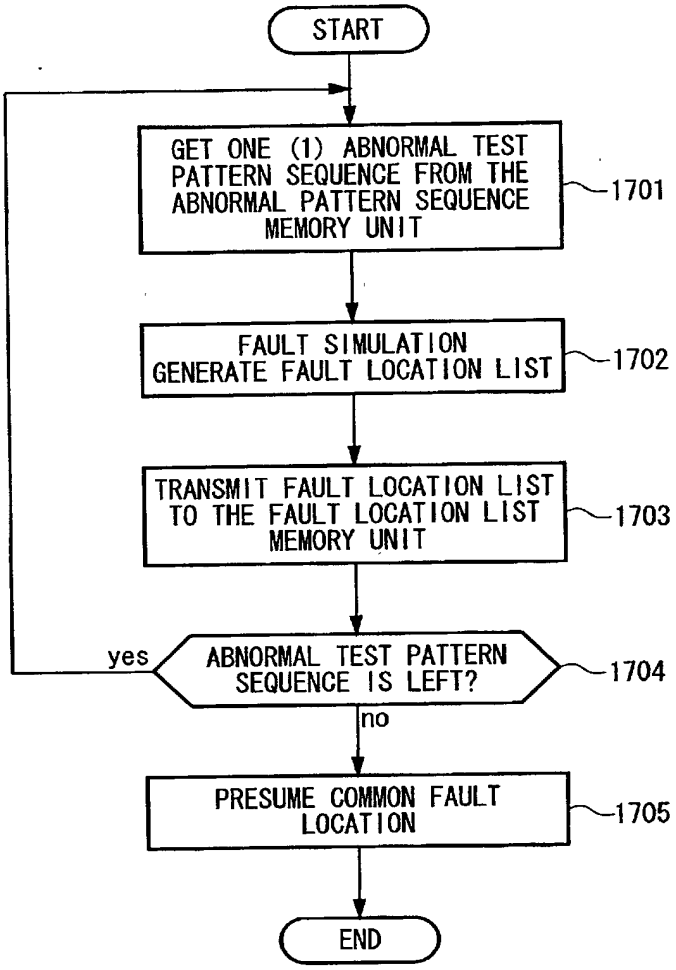

START
GET ONE (1) ABNORMAL TEST PATTERN SEQUENCE FROM THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
1701
FAULT SIMULATION GENERATE FAULT LOCATION LIST
1702
TRANSMIT FAULT LOCATION LIST TO THE FAULT LOCATION LIST MEMORY UNIT
1703
yes
ABNORMAL TEST PATTERN SEQUENCE IS LEFT?
1704
no
PRESUME COMMON FAULT LOCATION
1705
END

FIG. 36

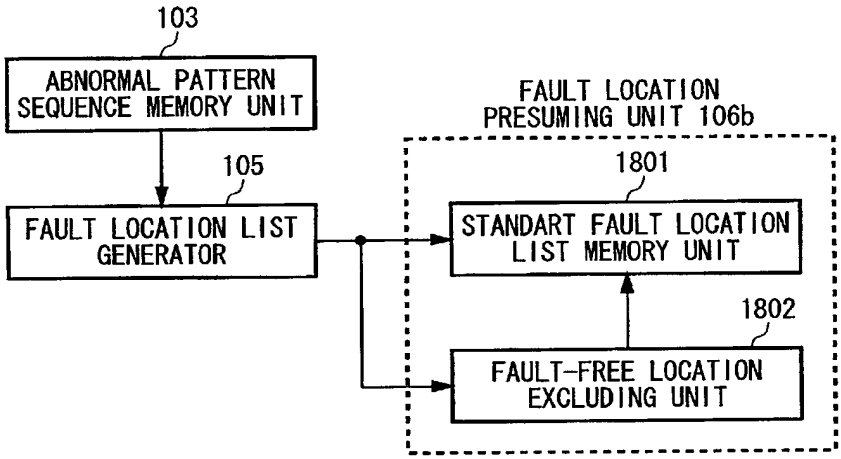

103
ABNORMAL PATTERN SEQUENCE MEMORY UNIT
105
FAULT LOCATION LIST GENERATOR
FAULT LOCATION PRESUMING UNIT 106b
1801
STANDART FAULT LOCATION LIST MEMORY UNIT
1802
FAULT-FREE LOCATION EXCLUDING UNIT

FIG. 37

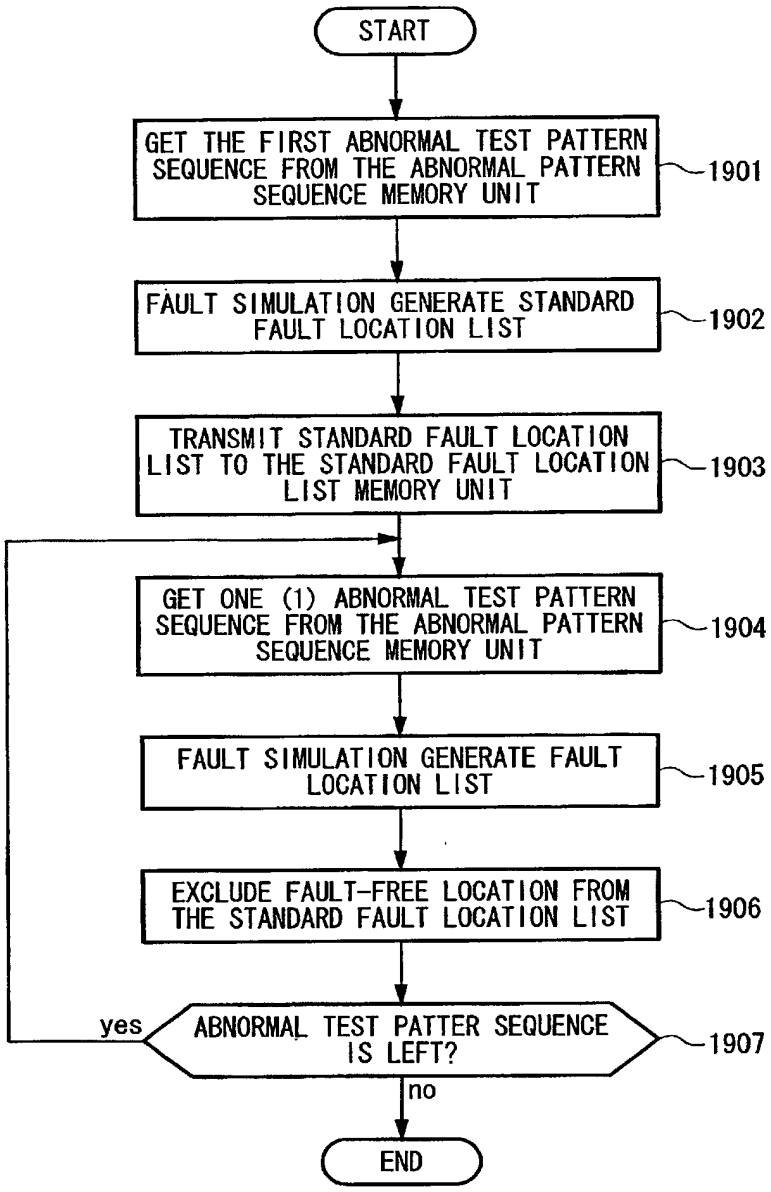

START
GET THE FIRST ABNORMAL TEST PATTERN SEQUENCE FROM THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
1901
FAULT SIMULATION GENERATE STANDARD FAULT LOCATION LIST
1902
TRANSMIT STANDARD FAULT LOCATION LIST TO THE STANDARD FAULT LOCATION LIST MEMORY UNIT
1903
GET ONE (1) ABNORMAL TEST PATTERN SEQUENCE FROM THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
1904
FAULT SIMULATION GENERATE FAULT LOCATION LIST
1905
EXCLUDE FAULT-FREE LOCATION FROM THE STANDARD FAULT LOCATION LIST
1906
yes
ABNORMAL TEST PATTER SEQUENCE IS LEFT?
1907
no
END

FIG. 38

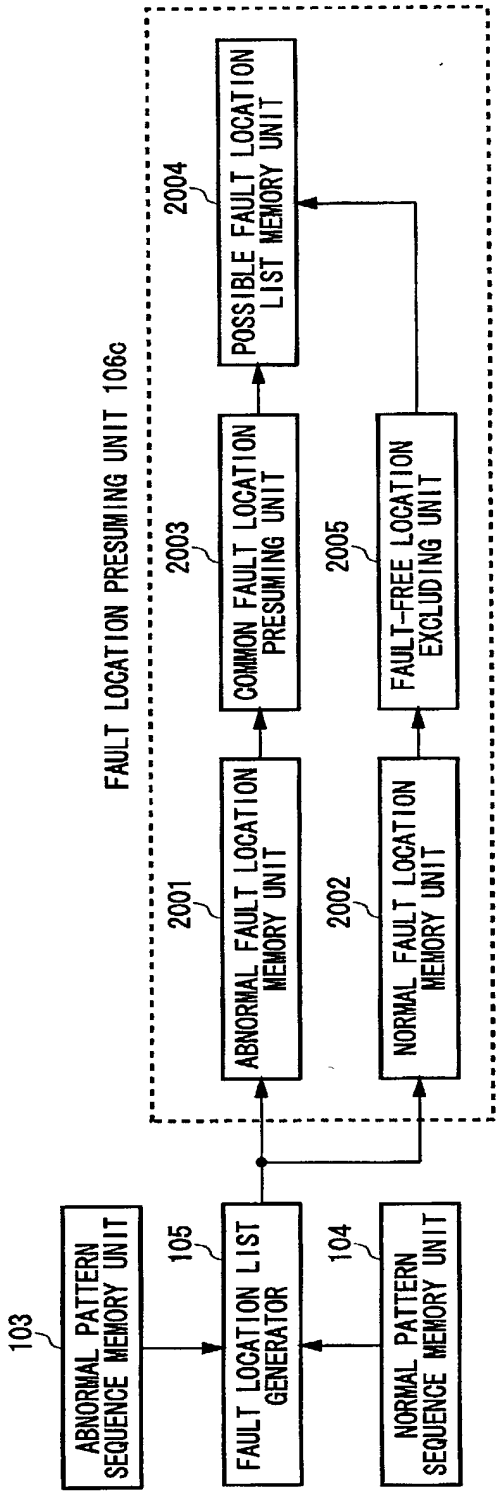

FAULT LOCATION PRESUMING UNIT 106c
ABNORMAL PATTERN SEQUENCE MEMORY UNIT
103
FAULT LOCATION LIST GENERATOR
105
NORMAL PATTERN SEQUENCE MEMORY UNIT
104
ABNORMAL FAULT LOCATION MEMORY UNIT
2001
NORMAL FAULT LOCATION MEMORY UNIT
2002
COMMON FAULT LOCATION PRESUMING UNIT
2003
FAULT-FREE LOCATION EXCLUDING UNIT
2005
POSSIBLE FAULT LOCATION LIST MEMORY UNIT
2004

FIG. 39

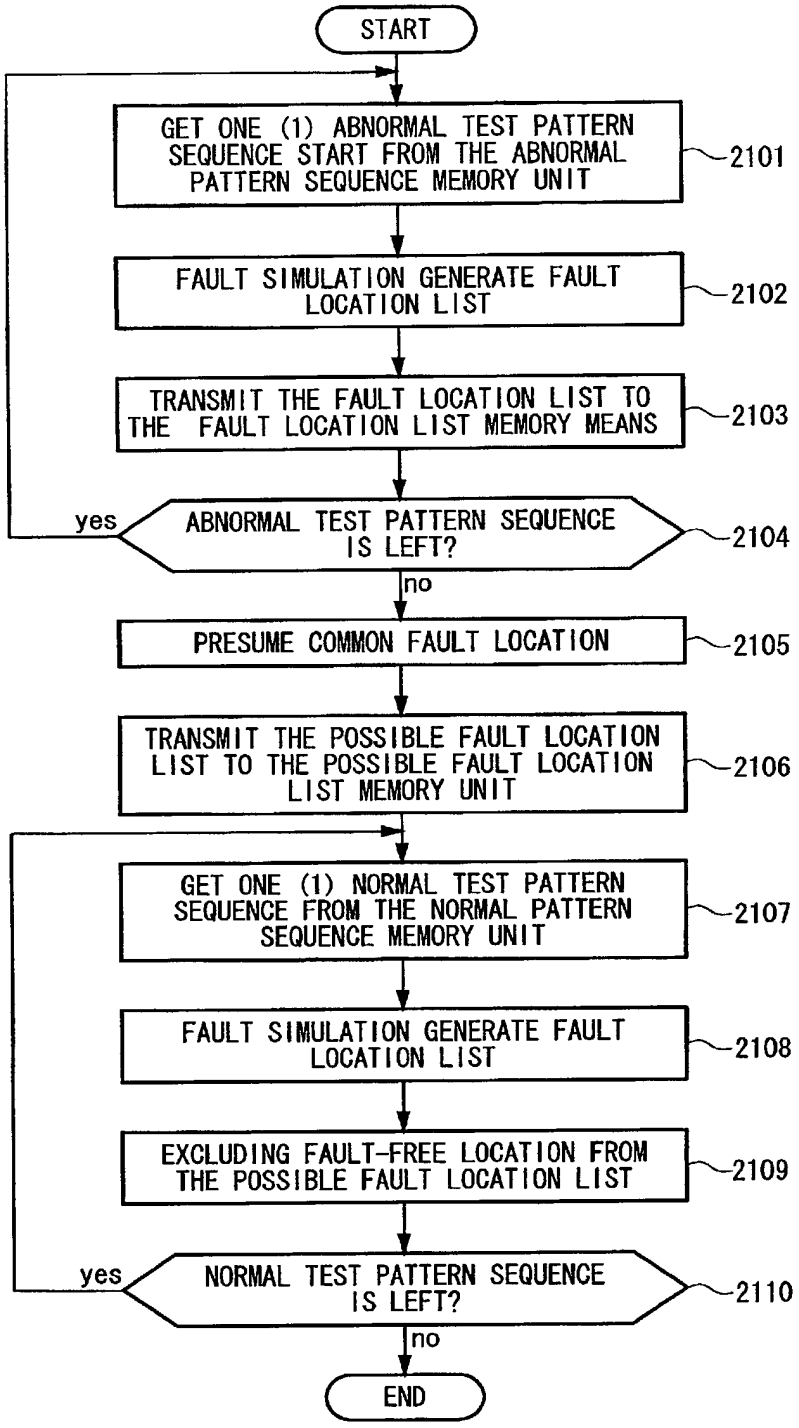

START
GET ONE (1) ABNORMAL TEST PATTERN SEQUENCE START FROM THE ABNORMAL PATTERN SEQUENCE MEMORY UNIT
2101
FAULT SIMULATION GENERATE FAULT LOCATION LIST
2102
TRANSMIT THE FAULT LOCATION LIST TO THE FAULT LOCATION LIST MEMORY MEANS
2103
yes
ABNORMAL TEST PATTERN SEQUENCE IS LEFT?
2104
no
PRESUME COMMON FAULT LOCATION
2105
TRANSMIT THE POSSIBLE FAULT LOCATION LIST TO THE POSSIBLE FAULT LOCATION LIST MEMORY UNIT
2106
GET ONE (1) NORMAL TEST PATTERN SEQUENCE FROM THE NORMAL PATTERN SEQUENCE MEMORY UNIT
2107
FAULT SIMULATION GENERATE FAULT LOCATION LIST
2108
EXCLUDING FAULT-FREE LOCATION FROM THE POSSIBLE FAULT LOCATION LIST
2109
yes
NORMAL TEST PATTERN SEQUENCE IS LEFT?
2110
no
END

FIG. 40